Amendments to the Specification

Amend the paragraph beginning on line 5 of page 2 as follows:

A1

The processors ~~1001~~ 100-1 through 100-n ~~sends~~ send the same message to both A-side node ~~230A~~ 200A and B-side node 200B ~~230B~~, in order to provide a duplex IPC path.

Amend the paragraph beginning on line 7 of page 2 as follows:

A2

Figure 2 is a block diagram of the construction of [[a]] duplex nodes (230A, 230B) ~~node~~ positioned at the switching device 200.

Amend the paragraph beginning on line 9 of page 2 as follows:

A3

The node A 230A and node B 230B are constructed ~~as the~~ in a redundancy duplex structure. ~~interfaces by means of the switching~~ Switching unit 210 ~~for switching~~ switches messages between the nodes and a D-BUS, and ~~interfaces by means of~~ the nodes are connected to the processors ~~and an~~ through a U-LINK. The duplex node A 230A and node B 230B receive messages from the processors through the U-LINK to thus relay the same to the D-BUS, and receives messages from the D-BUS to thus relay the same to the U-LINK. The message through the U-LINK is a 1 bit serial data, and the message through the D-BUS is a number of bits (for example, 8 bits or 16 bit or 32 bits) of parallel data.

Amend the paragraph beginning on line 3 of page 5 as follows:

A4

On the contrary, when a HDCL message is received from the D-BUS, the duplexing control unit ~~233c~~ 234 outputs a signal (DRX_Enable) to the DRX Interface 233c, and the DRX Interface outputs a signal (TX_START) informing that there is a message to be transmitted to hte corresponding processor to the TX buffer 231[[,]]. ~~and stores the~~ The message received through the D-BUS is stored in the TX buffer.

Amend the paragraph beginning on line 19 of page 5 as follows:

A5

The inactive node A 230-A ~~stop~~ stops the message relay function by disabling the node control unit ~~230~~ 233.

Amend the paragraph beginning at line 16 of page 8 as follows:

A6

Figure 5 is a block diagram of the construction of one ~~node~~ of a plurality of duplex nodes according to the present invention.

Amend the paragraph beginning at line 18 of page 8 as follows:

A7

As shown therein, the node according to the present invention includes a TX buffer 231, RX buffer 232, node control unit 233, and duplexing control unit 300. The TX buffer 231 performs the same function as the TX buffer 231 as shown in Figure 3, and it is different from that as in the conventional art in that a signal (TX _EMPTY) informing whether or not there is a message stored in the TX buffer 231 is outputted to the duplexing control unit 300. The RX buffer 232

perform the same function as the RX buffer 231 as shown in figure 3, and it is different from that as in the conventional art in that a signal (RX_EMPTY) informing whether or not there is a message stored in the RX buffer is outputted to the duplexing control unit 300. The node control unit [[232]] 233 is constructed in the same manner as the node control unit [[231]] 233 as shown in Figure 3, and it is different from that as in the conventional art in that a signal (TX_START) informing that there is a message to be transmitted from a DRX interface 233c is outputted to not only the TX buffer 231, but also the duplexing control unit 300 and moreover a signal(RX_START) informing that there is a message received from a URX interface 233b is outputted to not only the RX buffer 232, but also the duplexing control unit 300.

CONT A7